CLAIMS

What is claimed is:

1. A method comprising:

providing a first clock signal having a first frequency to a state machine counter;

providing a second clock signal having a second frequency that is an integer multiple of the first clock frequency to the state machine counter;

applying the first clock signal to reset the state machine counter to an initial state;

incrementing the state machine counter with the second clock signal wherein the state machine counter has an integer number of states equivalent to the ratio of the second clock signal frequency to the first clock signal frequency;

generating an intermediate clock signal with the state machine counter wherein the counter produces an output signal whenever the state machine increments through all states to return to the initial state; and

applying the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency.

2. The method of claim 1 wherein applying the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency further comprises:

delaying a data signal at the first clock frequency by two cycles of the second clock frequency;

reclocking the data signal at the first clock frequency to the intermediate clock; and

reclocking the data signal at the intermediate clock to the second frequency.

3. The method of claim 1 wherein the applying the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency further comprises:

reclocking a data signal at the second clock frequency to the intermediate clock;

delaying the data signal at the intermediate clock by one cycle of the second clock frequency; and

reclocking the data signal at the intermediate clock to the first clock frequency.

4. The method of claim 1 further comprising:

providing the second clock signal to a second state machine counter;

providing a third clock signal having a third frequency that is an integer fraction of the first clock frequency to the second state machine counter;

applying the second clock signal to reset the second state machine counter to an initial state;

incrementing the second state machine counter with the third clock signal wherein the second state machine counter has an integer number of states equivalent to the ratio of the second clock frequency to the third clock frequency;

generating a second intermediate clock signal with the second state machine counter wherein the second state machine counter produces an output signal whenever the state machine increments through all possible states and returns to the initial state; and

applying the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency.

5. The method of claim 4 wherein the applying the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency further comprises:

delaying a data signal at the second clock frequency by two cycles of the third clock frequency;

reclocking the data signal at the second clock frequency to the second intermediate clock frequency; and

reclocking the data signal at the second intermediate clock frequency to the third frequency.

6. The method of claim 5 wherein data at the first clock frequency is synchronized to data at the third clock frequency by first synchronizing data to the second clock frequency then synchronizing the data at the second clock frequency to the third clock frequency.

7. The method of claim 4 wherein the applying the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency further comprises:

reclocking a data signal at the third clock frequency to the second intermediate clock;

delaying the data signal at the second intermediate clock by one cycle of the third clock frequency; and

reclocking the data signal at the second intermediate frequency to the second clock frequency.

8. The method of claim 7 wherein data at the first clock frequency is synchronized to data at the third clock frequency by first synchronizing the data to the second clock frequency then synchronizing the data at the second clock frequency to the third clock frequency.

9. The method of claim 1 wherein the state machine counter generates a precursor intermediate clock signal that is one period of the second clock frequency ahead of the intermediate clock signal.

10. The method of claim 9 further comprising:

distributing the precursor intermediate clock signal to different locations;

latching the precursor intermediate clock signal to a local second clock signal to generate a distributed intermediate clock signal; and,

synchronizing data at different locations using the distributed intermediate clock signal.

11. A product comprising:

instructions to direct a processor to provide a first clock signal having a first frequency to a state machine counter, provide a second clock signal having a second frequency that is an integer multiple of the first clock frequency to the state machine counter, apply the first clock signal to reset the state machine counter to an initial state, increment the state machine counter with the second clock signal wherein the state machine counter has an integer number of states equivalent to the ratio of the second clock signal frequency to the first clock signal frequency, generate an intermediate clock signal with the state machine counter wherein the counter produces an output signal whenever the state machine increments through all states to return to the initial state, and, apply the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency, and;

machine readable media to store the instructions.

12. The product of claim 11 wherein the instructions to apply the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency further comprises instructions to:

delay a data signal at the first clock frequency by two cycles of the second clock frequency,

reclock the data signal at the first clock frequency to the intermediate clock, and,

reclock the data signal at the intermediate clock to the second frequency.

13. The product of claim 11 wherein the instruction to apply the intermediate clock signal to synchronize data between the first clock frequency and the second clock frequency further comprises instructions to:

reclock a data signal at the second clock frequency to the intermediate clock,

delay the data signal at the intermediate clock frequency by one cycle of the second clock frequency, and,

reclock the data signal at the intermediate clock to the first clock frequency.

14. The product of claim 11 further comprising:

instructions to provide the second clock signal to a second state machine counter, provide a third clock signal having a third frequency that is an integer fraction of the first clock frequency to the second state machine counter, apply the second clock signal to reset the second state machine counter to an initial state, increment the second state machine counter with the third clock signal wherein the second state machine counter has an integer number of states equivalent to the ratio of the second clock frequency to the third clock frequency, generate a second intermediate clock signal with the second state machine counter wherein the second state machine counter produces an output signal whenever the state machine increments through all possible states and returns to the initial state, and, apply the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency, and;

machine readable media to store the instructions.

15. The product of claim 14 wherein the instructions to apply the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency further comprise instructions to:

delay a data signal at the second clock frequency by two cycles of the third clock frequency;

reclock the data signal at the second clock frequency to the second intermediate clock; and

reclock the data signal at the second intermediate clock to the third frequency.

16. The product of claim 15 wherein data at the first clock frequency is synchronized to data at the third clock frequency by first synchronizing data to the second clock frequency then synchronizing the data at the second clock frequency to the third clock frequency.

17. The product of claim 14 wherein the instructions to apply the second intermediate clock signal to synchronize data between the second clock frequency and the third clock frequency further comprise instructions to:

reclock a data signal at the third clock frequency to the second intermediate clock;

delay the data signal at the second intermediate clock frequency by one cycle of the third clock frequency; and

reclock the data signal at the second intermediate clock to the second clock frequency.

18. The product of claim 17 wherein data at the first clock frequency is synchronized to data at the third clock frequency by first synchronizing the data to the second clock frequency then synchronizing the data at the second clock frequency to the third clock frequency.

19. The product of claim 11 wherein the state machine counter generates a precursor intermediate clock signal that is one period of the second clock frequency ahead of the intermediate clock signal.

20. The method of claim 19 further comprising instructions to:

distribute the precursor intermediate clock signal to different locations,

latch the precursor intermediate clock signal to a local second clock signal to generate a distributed intermediate clock signal, and,

synchronize data at different locations using the distributed intermediate clock signal, and; machine readable media to store the instructions.

21. An apparatus comprising:

a first data processing device clocked at a first frequency;

a second data processing device clocked at a second frequency that is an integer multiple of the first frequency;

instructions to direct a processor to provide a first clock signal having the first frequency to a state machine counter, provide a second clock signal having the second frequency to the state machine counter, apply the first clock signal to reset the state machine counter to an initial state, increment the state machine counter with the second clock signal wherein the state machine counter has an integer number of states equivalent to the ratio of the second clock signal frequency to the first clock signal frequency, generate an intermediate clock signal with the state machine counter wherein the counter produces an output signal whenever the state machine increments through all states to return to the initial state, and, apply the intermediate clock signal to synchronize data between the first data processing device and the second data processing device, and;

machine readable media to store the instructions.

22. The apparatus of claim 21 wherein the instructions to apply the intermediate clock signal to synchronize data between the first data processing device and the second data processing device further comprises instructions to:

delay a data signal at the first clock frequency by two cycles of the second clock frequency,

reclock the data signal at the first clock frequency to the intermediate clock, and,

reclock the data signal at the intermediate clock to the second frequency.

23. The apparatus of claim 21 wherein the instruction to apply the intermediate clock signal to synchronize data between the first data processing device and the second data processing device further comprises instructions to:

reclock a data signal at the second clock frequency to the intermediate clock,

delay the data signal at the intermediate clock by one cycle of the second clock frequency, and,

reclock the data signal at the intermediate clock to the first clock frequency.

24. The apparatus of claim 21 further comprising:

a third data processing device clocked at a third frequency that is an integer fraction of the first clock frequency;

instructions to provide the second clock signal to a second state machine counter, provide a third clock signal having the third frequency to the second state machine counter, apply the second clock signal to reset the second state machine counter to an initial state, increment the second state machine counter with the third clock signal wherein the second state machine counter has an integer number of states equivalent to the ratio of the third clock frequency to the second clock frequency, generate a second intermediate clock signal with the second state machine counter wherein the second state machine counter produces an output signal whenever the state machine increments through all states and returns to the initial state, and, apply the second intermediate clock signal to synchronize data between the second data processing device and the third data processing device, and; machine readable media to store the instructions.

25. The apparatus of claim 24 wherein the instructions to apply the second intermediate clock signal to synchronize data between the second data processing device and the third data processing device further comprise instructions to:

delay a data signal at the second clock frequency by two cycles of the third clock frequency;

reclock the data signal at the second clock frequency to the second intermediate clock frequency; and

reclock the data signal at the second intermediate clock frequency to the third frequency.

26. The apparatus of claim 25 wherein data is synchronized between the first data processing device and the third data processing device by first synchronizing data between the first data processing device and the second data processing device then synchronizing the data between the second data processing device and the third data processing device.

27. The apparatus of claim 24 wherein the instructions to apply the second intermediate clock signal to synchronize data between the second data processing device and the third data processing device further comprise instructions to:

reclock a data signal at the third clock frequency to the second intermediate clock;

delay the data signal at the second intermediate clock by one cycle of the third clock frequency; and

reclock the data signal at the second intermediate clock to the second clock frequency.

28. The apparatus of claim 27 wherein data is synchronized between the first data processing device and the third data processing device by first synchronizing data between the first data processing device and the second data processing device then synchronizing the data between the second data processing device and the third data processing device.

29. The apparatus of claim 21 wherein the state machine counter generates a precursor intermediate clock signal that is one period of the second clock frequency ahead of the intermediate clock signal.

30. The apparatus of claim 19 further comprising instructions to:

distribute the precursor intermediate clock signal to different locations,

latch the precursor intermediate clock signal to a local second clock signal to generate a distributed intermediate clock signal, and,

synchronize data at different locations using the distributed intermediate clock signal, and; machine readable media to store the instructions.